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PLAN-BASED EVALUATION OF DESIGNS FOR MICROWAVE MODULES[1]

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ABSTRACT

This paper describes EDAPS, an integrated system for designing and planning the manufacture of microwave modules. Microwave modules are complex devices having both electrical and mechanical properties, and EDAPS integrates electrical design, mechanical design, and process planning for both the mechanical and electrical domains.

Since EDAPS generates process plans concurrently with design, we are developing ways for EDAPS to provide feedback about manufacturability, cost, and lead time to the designers, based on the process plans to be used in the manufacture of their designs.

1 MOTIVATION

One of the primary motivations for Integrated Product and Process Design (IPPD) is the observation that 70% to 80% of manufacturing cost is determined while the product is being designed [34]. In order to avoid expensive and time-consuming *design-manufacture-test-redesign* cycles, it is important to address design and manufacturing issues concurrently.

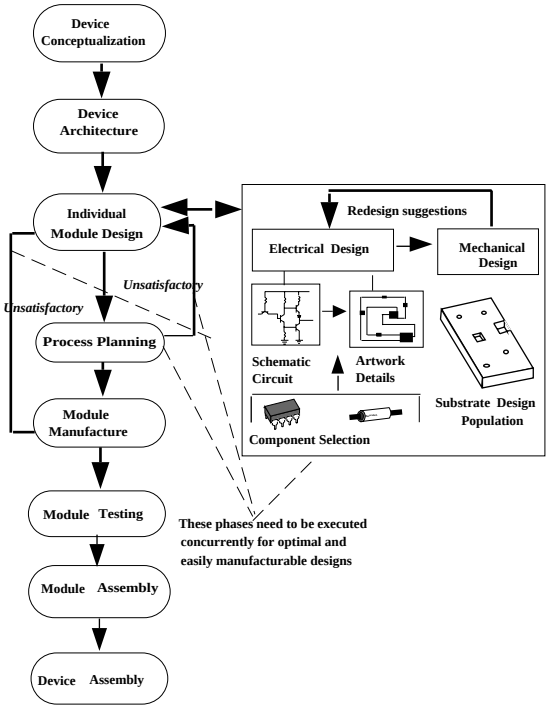

Figure 1. Design and manufacturing cycle for microwave modules.

One approach to IPPD is to develop interdisciplinary teams of designers, engineers and manufacturing personnel to address design and manufacturing issues concurrently during the design stage [12]. For the design of complex products, this will require designers from all relevant specialities to work closely with the product development team.

As an example, consider the design and manufacture of com-

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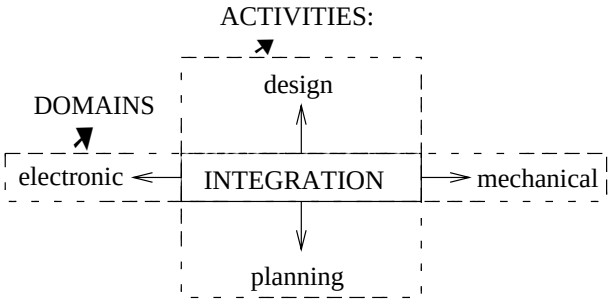

Figure 2. Integration of disciplines for the design and manufacture of complex electromechanical devices.

plex electro-mechanical devices such as *microwave modules* (described further in Section 3). Figure 1 illustrates the design and manufacturing cycle for microwave modules, which is highly interdisciplinary in nature. Electronic designers develop the detailed circuitry; mechanical designers design the device to resist shock and vibrational loadings, and develop the assemblies, the heat removal systems, and the housing of the device; and manufacturing engineers apply electronic manufacturing processes (such as lithography, soldering, cleaning, and testing), and mechanical manufacturing processes (such as drilling and milling) to manufacture the end product.

In the design of complex products that include microwave modules and other electro-mechanical devices as subsystems, achieving IPPD requires coordinating a large interdisciplinary team. In large organizations, this can be a difficult task [26].

The task of communicating design and manufacturing requirements and design changes across disciplines could be greatly aided by a carefully designed computer system that integrates both electronic and mechanical computer-aided design (CAD) tools, and provides access to process planning and design evaluation capabilities, as shown in Figure 2. Such a system could be used for designing both the electronic and mechanical aspects of a product, analyzing various aspects of the design's performance, planning how to manufacture the proposed design, and evaluating the process plans to provide feedback to the designer.

Few existing computer systems can successfully address all of these issues in a single integrated environment—and there are several open questions about the best way to design such a system. To explore these issues, we have created *Electro-mechanical Design And Planning System (EDAPS)*, a toolkit for microwave module manufacture that integrates electronic and mechanical computer-aided design, electronic and mechanical process planning, and plan-based design evaluation. EDAPS generates process plans concurrently with design, and assists the designer in performing plan-based critiquing of microwave module designs. EDAPS performs process planning both in the mechanical domain, including such processes as drilling and milling; and in the electronic domain, including such processes as via plating, artwork deposition, placing components, and soldering. Thus, EDAPS can provide feedback about manufacturability, cost, and lead time to the designers, based on process plans for the manufacture of the device.

2 RELATED RESEARCH

There have been a number of efforts in the direction of achieving IPPD practices in industry. Initial efforts were focused on establishing guidelines to inform designers of manufacturing and assembly concerns to be addressed at the design stage [5, 4, 2].

With the popular use of CAD tools for design activities, more and more CAD systems started incorporating manufacturability analysis modules that helped designers make intelligent decisions and reduce the manufacturing errors and difficulties of their designs. Using design for assembly guidelines, Jakiela and others [19] built a rule-based Design-For-Assembly system that gives feedback about assemblability when the designer adds new features to the design. Another rule-based manufacturability system was developed by Ishii [21]. Gupta and others [15] have developed IMACS, which generates the best operation plans for machined components and gives feedback about manufacturing infeasibilities in the design. However, none of these tools are applicable to the electronic domain.

In the electronic domain, Harhalakis and others [16] have developed a rule-based system for critiquing the manufacturability of microwave modules. However, this system is not directly linked to an electronic or mechanical CAD system. Feldmann and others [14] describe a system that integrates electronic and mechanical CAD tools for three-dimensional molded printed circuit boards, where circuits are no longer in planar configurations. However, these tools and systems do not evaluate the designs with respect to cost and lead times.

Commercially, several CAD tools are available for electronic circuitry design (such as Mentor Graphics, OrCAD, EEsof, and MAGIC). These electronic CAD packages automatically check design rules, and some even perform manufacturing yield analysis of the design [13]. However, since these packages use a two-dimensional representation of the design, they neither represent three-dimensional mechanical features nor perform any sort of mechanical feasibility and manufacturability analysis on devices. Such tasks would require a three-dimensional solid-model representation of the design.

Process planning can be defined as the act of preparing detailed operating instructions that transform an engineering design to a final part [8]. *Computer-Aided Process Planning (CAPP)* systems have been traditionally classified as *variant* or *generative*. In the variant approach, new designs are matched with old designs whose process plans are stored in the database. Process plans for the matching old designs are retrieved and manually modified to suit the manufacturing of the new design. Thus, a degree of human involvement is necessary in generating the

plans. In the generative approach, decisions needed to convert the stock to final design specifications are automatically taken by the computer by means of process knowledge, logic that performs geometric reasoning on the part, and other decision logic that is built into the system. A comprehensive review of numerous CAPP systems in the mechanical engineering domain that have been built to date can be found in [32].

Some efforts have focused on CAPP for electronic applications (for a review, see [24]). The PWA-Planner [9] is a rule-based system that performs planning for assembly of components on placement machines. Sanii [31] and others have taken Artificial Intelligence (AI) approaches to developing plans for assembling PCBs. However, none of these systems incorporate many manufacturing processes in the mechanical engineering domain, nor do they not provide feedback to the designer. Young and others [23] have developed a process planning and concurrent engineering system for PCBs that represents process knowledge as constraints and provides manufacturability feedback on the design. However, since PCB manufacturing usually does not involve traditional manufacturing practices such as milling, they do not consider these processes; their process planning is not integrated with an electronic/mechanical CAD system; and they do not evaluate their plans for cost.

For classifying electro-mechanical designs, Candadai and others [7] have taken a Group-Technology-based approach. Based on this classification, Lam [22] generates high level process plans for the manufacture of these designs. Though Lam's system considers the manufacturing processes in both domains, it does not work concurrently with an electronic CAD tool.

The DARPA/MADE program focuses on achieving IPPD goals in the manufacture of Complex Electro-Mechanical (CEM) devices [38]. CEM devices, such as optical cameras and CD-ROMs, are more complex than the devices considered in this paper. As part of MADE, the SHARE project [36] examines how information technology tools could be applied to promote collaboration between design teams.

Trade-off analysis is an important part of design evaluation whenever designs can be evaluated according to more than one criterion, such as in the electro-mechanical domain. The MSDA advisor is a software tool that evaluates system level trade-offs between physical size, weight, thermal characteristics, reliability, cost, performance, and so forth in the selection of packaging technologies for components used in PCBs and ceramic substrates. This tool has been used to perform trade-offs [30].

3 MICROWAVE MODULES

3.1 Introduction

Most commercial electronic products operate in the 10kHz–1GHz radio frequency spectrum. However, in the telecommunications arena, the range of operation frequency has been increasing at a tremendous pace. For scientific and commercial long-range defense applications—such as radar, satellite communications, and long-distance television and telephone signal transmissions—radio frequencies prove unsuitable, primarily due to the high noise-to-signal ratio associated with radio frequencies. Moreover, the lower-frequency bands have become overcrowded due to the overuse of these bands for commercial communications applications [37].

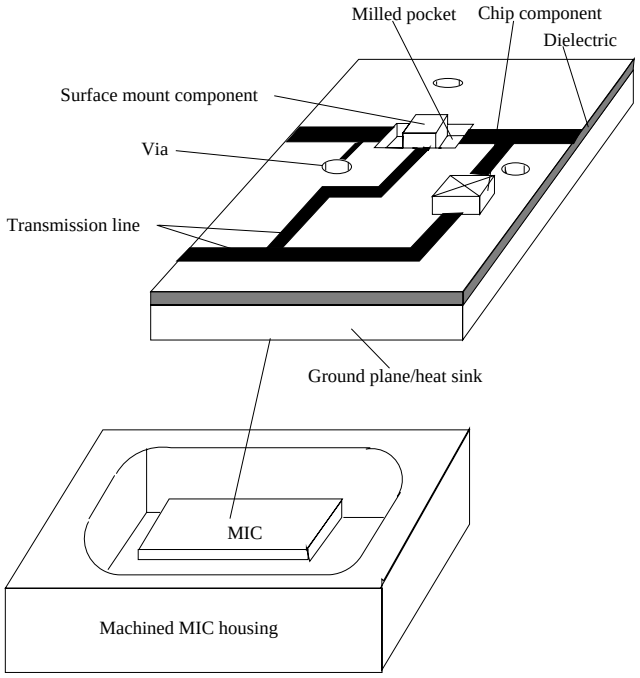

Figure 3. A typical microwave module, consisting of the MIC substrate, and its housing.

Consequently, in contrast to other commercial electronic products, most modern telecommunications systems operate in the 1–20 GHz microwave range, and modules of such systems are termed *microwave modules* (see Figure 3).

3.2 Terminology

In earlier microwave circuit assemblies, different parts of the circuit were built separately using *coaxial cables* or *waveguides*, and later assembled by screwing the parts together. Owing to the size and configuration of the coaxial cables and waveguides, the assemblies were significantly large, and the assembly procedure was time-consuming and clumsy. These earlier assemblies were replaced by *Microwave Integrated Circuits (MICs)*, where all functional components of the circuit are fabricated as *artwork* on the same planar board, using the same fabrication technology. In MICs, functional components such as transistors, resistors, and capacitors can be classified as either "integrated" or "hybrid".

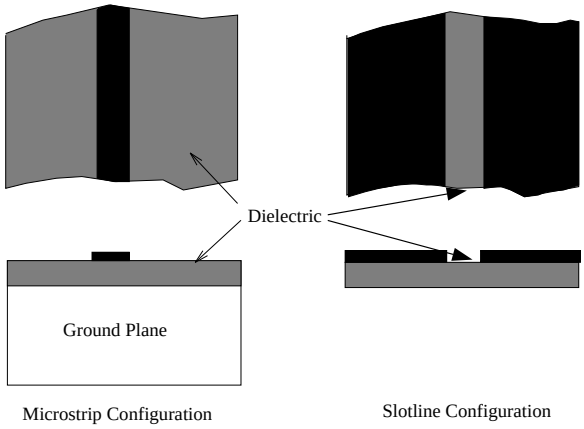

Figure 4. Transmission lines in microwave manufacturing.

Integrated components are fabricated as a geometric manifestation of the artwork. *Hybrid* components are assembled separately using techniques such as soldering, wire bonding, and ultrasonic bonding. If all functional elements of the device are integrated, such devices are known as *Monolithic Microwave Integrated Circuits (MMICs)*.

We will use the following terms throughout the paper (see Figure 3 and Figure 4 for illustrations):

- The *dielectric* is the substrate on which the artwork is laid out, and on which the hybrid components are assembled. The dielectric serves as a wave-conducting medium. Common materials used are PTFE (Teflon), polyolefin and aluminum-oxide ceramic.
- The *ground plane* is a metallic layer on top of which the dielectric layer resides. The ground plane is usually made of copper or aluminum. It provides grounding for the circuit, mechanical strength for the device, and acts as a medium to conduct away heat generated by the device. Hybrid components are mounted, and machined features such as milled pockets and drilled holes are developed on this plane.
- The *artwork* is a layer of etched circuit pattern containing traces, pads to mount hybrid components, components that are directly fabricated on the circuit, fiducials, and reference text elements. Usually, the artwork forms the topmost layer of the dielectric.
- *Transmission lines* are traces that carry energy to different parts of the circuit. Figure 4 illustrates some of the possible configurations of transmission lines. The Microstrip configuration is the simplest to manufacture.
- *Vias* are through-holes in the dielectric that carry electrical signals from the upper layer to the ground plane on the bottom side. Vias also conduct heat from the artwork layers to the heat sink.
- *Surface-mount components* are hybrid elements that are assembled on the surface of the dielectric. The leads of these components do not go into the dielectric, as opposed to the leads of through-hole components (which go through the surface).
- *Mounting features* are usually milled pockets that are used as a recess in which surface mount components sit. These pockets are especially necessary for components that dissipate high heat, because these components need to be directly connected to the heat sink. Such components include Gunn diodes and Impatt diodes.
- The *housing* is a cast, or machined, metallic enclosure which envelopes the entire assembled device. These enclosures are needed to provide electronic isolation of the devices; to provide rigidity and strength; to make external connections easy; and to dissipate the heat conducted from the device heat sinks.

3.3 Electronic Manufacturing Processes

The production method used for MICs depends on several factors, some of which are the choice of dielectric material, and the degree of integration of functional elements in the design. If all elements are assembled as hybrids, then lamination, photomask deposition, etching, plating, adhesive deposition, application of flux, reflow soldering, trimming, cleaning, testing, tuning, drilling, milling, and casting form a superset of the operations used [10, 6]. If, however, some components are fabricated as integrated elements, thin film and thick film deposition techniques must be used in addition [17]. In this work, we assume that the modules are fabricated as hybrid-only microstrip MICs, so that the thin/thick film processes can be avoided.

4 SYSTEM ARCHITECTURE

In the EDAPS system, we want to provide the designer with CAD tools for electronic and mechanical design, and with an integrated process planner for manufacturing processes both in the mechanical domain and in the electronic domain. Thus, as illustrated in Figure 5, the EDAPS system consists of three modules that can be invoked from a common user interface:

- In EDAPS's *circuit schematic and circuit layout module*, the designer generates electronic circuitry. An integrated set of packages supplied by EEsof's Series IV [13] software forms the core of this module. On top of this, we have developed routines to provide us with application specific information. We address the circuit layout module in more detail in Section 4.1.
- In EDAPS's *substrate design module*, the designer develops mechanical features of the MIC. Bentley System's Microstation CAD software application [25] supplies the set of tools required to achieve this functionality. We are developing routines in C++ and the Microstation Development Language

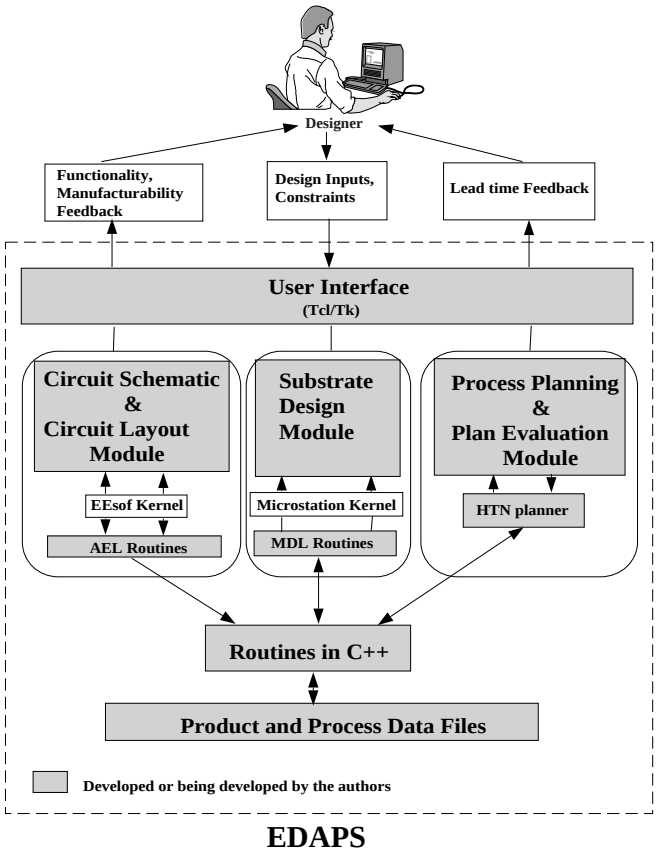

Figure 5. System architecture.

to integrate Microstation with the rest of the system and to extract and supply relevant manufacturing information to individual modules. We address the substrate design module in more detail in Section 4.2.

- In the *process planning and plan evaluation module*, an AI-based process planner that we are developing creates a process plan for the design, and reports to the designer the cost and lead time for the design. We address the process planning and plan evaluation module in more detail in Section 4.3.

The coordination of these modules and the exchange of data among them takes place through a user interface written in the *Tcl/Tk* language [27]. This user interface allows the designer to smoothly interact with the heterogeneous modules that constitute the system.

4.1 Circuit Schematic and Circuit Layout Module

For microwave circuit design and layout, EDAPS uses a powerful set of tools included in the EEsof electronic CAD tool [13]. In particular, EDAPS uses EEsof's Libra tool for linear and nonlinear schematic circuit design, and EEsof's ACADEMY tool for layout generation.

Using Libra, the designer designs the "schematic circuit", choosing components from pre-defined and user-defined device libraries. In *schematic circuits*, the components and transmission lines are represented as symbols. The actual artwork shapes corresponding to the circuit elements are not represented in the schematic. The designer subjects this circuit to time/frequency domain response analyses to achieve the desirable functionality. The designer does several design iterations, and Libra evaluates each design until the designer obtains a functionally satisfactory circuit. Figure 6 illustrates the schematic circuit of an oscillator designed with Libra.

Libra incorporates some design-for-manufacturing principles. Based on the required circuit functionality, the limiting tolerances on each component's electrical parameters can be calculated and thus manufacturing yield can be predicted. Yield information calculated this way gives an idea of the required investment in post production. This yield metric is the maximum yield that can be expected out of the design. It is useful in performing sensitivity analysis of the design. However, manufacturing yields are not only a function of electrical parameter tolerances. Some of the other influences can be the defects that result from the soldering processes that are directly related to the package shape, dimensions and materials.

Once the schematic circuit is complete, the artwork shapes necessary to realize circuit interconnections and other metalizations on the substrate are automatically generated by ACADEMY. The layout can also be interactively laid down to fit the artwork within specified size constraints, and to incorporate those artwork layer elements that do not have electronic significance. Examples of such elements are product identification numbers, design version numbers, fiducial marks, and the global origin for the microwave module. Figure 7 illustrates the layout for the oscillator designed earlier.

We have built routines in the *Application Extension Language (AEL)* supplied by EEsof to extract parts list from the design database. We have built routines in C++ to query the design database and obtain component parameters and artwork details.

To facilitate the conversion between EEsof generated layout and external CAD systems supplied by different vendors, ACADEMY provides several import/export translators. Conversions to and from popular formats such as Gerber (for direct photo-mask generation), HPGL/2 (for printing/plotting), DXF (AutoCAD format), and the ANSI standard IGES neutral file format [18] are supported. In order to develop mechanical features of the MIC, we convert layout data into the IGES format for export to the mechanical CAD system described in Section 4.2. Another routine written in C++ handles this translation.

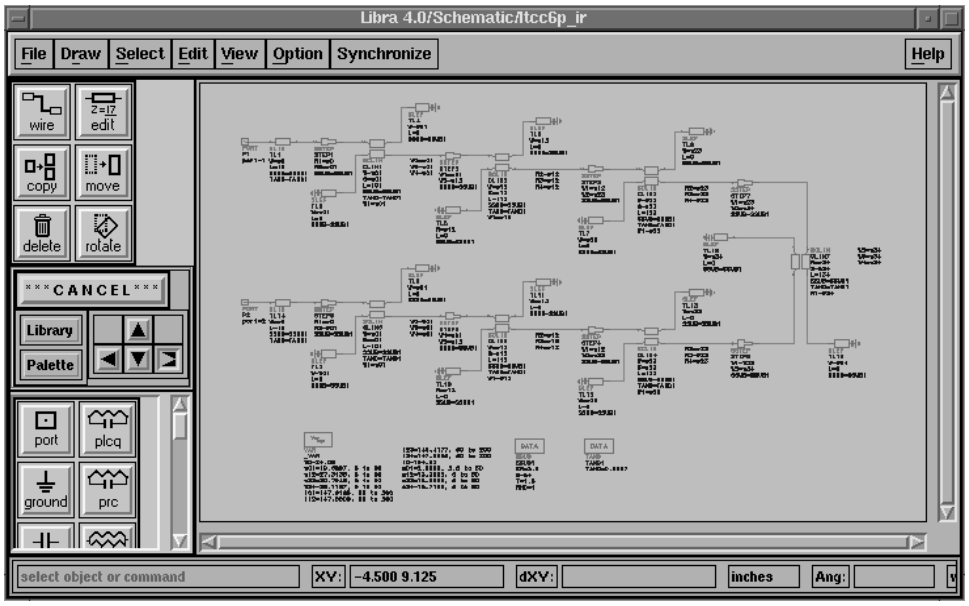

Figure 6. Schematic circuit design using Libra.

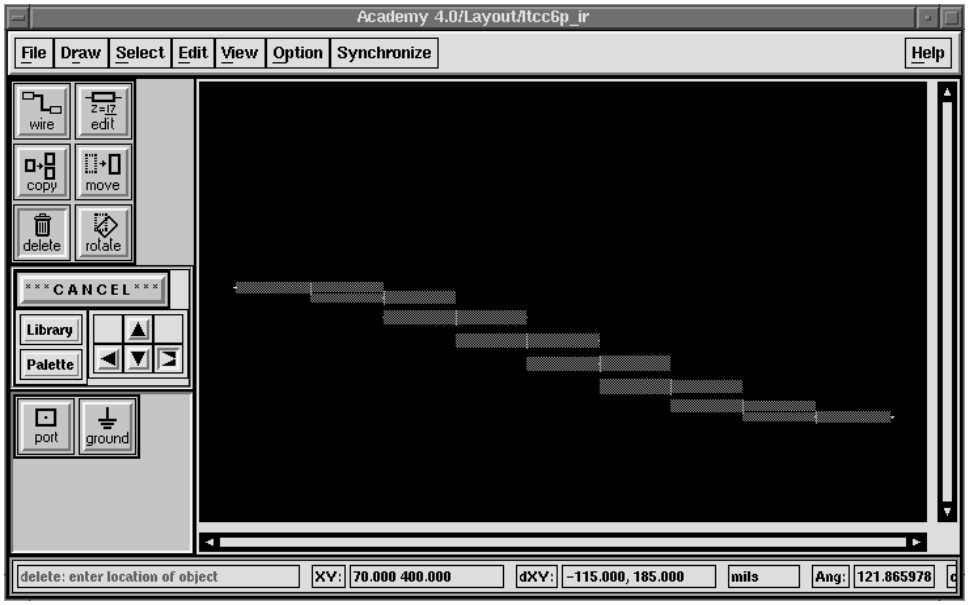

Figure 7. Layout generated by ACADEMY.

4.2 Substrate Design Module

The substrate design module is being built using MicroStation, a comprehensive CAD package supplied by Bentley Systems Inc. Microstation modeler is a parametric *feature-based design system*. According to Salomons [29], features are information sets that refer to aspects of form and other attributes of a part, such that these sets can be used in reasoning about the design, performance or manufacture of the part or assemblies they constitute. Features in Microstation are represented as nodes of the design tree. Nodes in the feature tree are created in the order they were built into the design by the designer. The ACIS [1] solid modeler is used internally to represent and provide methods to generate and modify features defined in Microstation.

Several manufacturing applications prefer to work with *manufacturing features* that contain information helpful in reasoning about manufacturing feasibility, cost, time, and so on. In EDAPS,

the manufacturing features that are most relevant to process planning and plan evaluation are:

- *Dielectric* : The dielectric is assumed to have cuboidal geometry with a designer specified corner radii, thereby directly corresponding to the material removal shape volumes of end-milling features. The feature information set contains dimensions, corner radii, location, orientation, and electronic parameters such as the dielectric constant and dielectric material.
- *Heat Sink*: The geometry of this feature is again assumed to be cuboidal with corner radii; each heat sink directly corresponds to an end-milling feature. The feature information set contains its material, length, width, height and corner radius. An additional constraint specifies that the widths and lengths of the heat sink and dielectric be equal, since the dielectric is fabricated on the heat sink.
- *Component Mounting Pockets*: For packaged components that require recess in the substrate for mounting and grounding, component mounting pocket features whose geometry corresponds to an end-milling feature have been provided. By default, the dimensions of this feature are a function of the dimensions of the packaged component, and its location is the same as that of the packaged component. This generic end-milling feature can be used to construct all other cutouts, pockets, and grooves in the dielectric and heat sink.
- *Vias*: Vias are represented as manufacturing features because they directly correspond to the material removal volumes of drilling features. In addition to diameter, location, orientation, and length of the vias, useful manufacturing information such as electroplating thickness if electroplated, and if tapped, a reference to the pitch, nominal diameter and the owner screw will be stored in this feature.

4.3 Process Planning and Plan Evaluation Module

To perform process planning for microwave module designs, we use an approach from artificial intelligence called *hierarchical task-network* (HTN) planning [11, 28, 35, 39]. We have also used this approach in some of our other work [33].

HTN planning proceeds by taking a complex *task* to be performed and considering various *methods* for accomplishing the task. Each method provides a way to decompose the task into a set of smaller tasks. By applying other methods to decompose these tasks into even smaller tasks, the planner will eventually produce a set of primitive tasks that it can perform directly.

As an example, one method for making the artwork for the MIC is to do the following series of tasks: precleaning for the artwork, followed by application of photoresist, followed by photolithography for the artwork, followed by etching. There are several alternative methods for applying photoresist: spindling the photoresist, spraying on the photoresist, painting on the photoresist, and spreading out the photoresist from a spinner. This

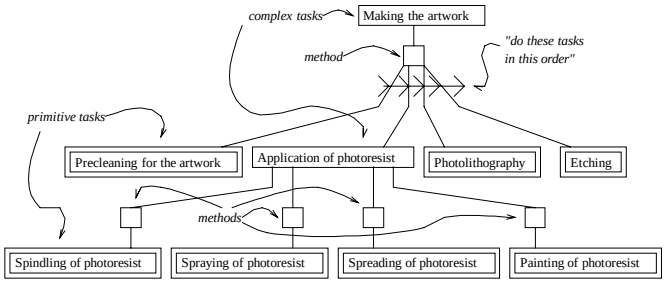

Figure 8. Part of the task network for microwave module manufacture.

relationship between tasks and methods results in a *task network*, part of which is shown in Figure 8.

This decomposition of tasks into various subtasks is important for process planning for the manufacture of microwave modules for two reasons. First, the decomposition in an HTN naturally corresponds to the decomposition of a MIC into the parts and processes required to manufacture it. Second, the ability to include the complex tasks "make drilling and milling features", "make artwork", "assembly and soldering", and "testing and inspection" in sequence provides a uniform framework that can naturally accommodate all the processes in mechanical and electronic manufacturing.

Sometimes a particular method can always be used to perform a particular task. For example, because spreading out the photoresist from a spinner is so accurate, this method can always be used to perform the task of applying the photoresist. Sometimes a particular method can only sometimes be used to perform a particular task. For example, because spraying on the photoresist is only somewhat accurate, this method cannot be used to apply the photoresist if a coupler in the artwork has a gap of less than or equal to 10 mils.

Certain tasks are *primitive*, meaning that they do not break down into any other tasks. We consider a task to be primitive if it is considered to be a single small step in the manufacturing process. For example, precleaning for the artwork is a primitive task. Once the complex task of making the entire MIC has been broken down into a series of primitive tasks, a process plan has been created; carrying out the steps of the process plan will result in the creation of the MIC.

The planning module constructs a set of process plans, and evaluates them to see which takes the least amount of time. In some cases, it evaluates a set of incomplete process plans and discards all but the one which takes the least amount of time. For example, because the method of application for photoresist does not affect the method of application for solder paste, if the quickest method of applying photoresist is spraying it on, then there is no need to generate process plans in which some other method of application is used. If no process plans can manufacture the device—because some manufacturability constraint,

```
Parts:
Block
 Dimensions: 7,4,1
 Ground material: Aluminum
 Substrate: Teflon
 Substrate thickness: 30 mils
 Metallized layer: Copper
 Metallized layer thickness: 7 mils
 Part number: 80280SA/2
Resistor
 Name: P1
 Part number: RNC55H237OFS
 Description: Motorola SS163
 Specification: MIL-R-55182
[...]
Processes:
Opn A  BC/WW  Setup  Run   LN  Description
001 A   VMC1    2.0  0.0   01  Hold substrate with
                               flat vise jaws at
                               3.5,4,0.5 and
                               3.5,0,0.5
                           02  Establish datum point
                               at 0,0,1
001 B   VMC1    0.0  0.6   01  Drill hole: 1,4,0
                               depth: 1 using
                               0.25 radius bit
                           02  Drill hole: 3,4,0
                               depth: 1 using
                               0.25 radius bit
001 C   VMC1    0.0  0.3   01  Drill hole: 3.5,6.5,0
                               depth: 1 using
                               0.125 radius bit
001 D   VMC1    0.0  5.0   01  Mill slot: 0.5,1,0
                               dimensions 3,1,1
                               using 0.5 radius
                               end-milling tool
001 T   VMC1    2.0  5.9   01  Total time on VMC1
```

Figure 9. Part of a process plan in a standard format.

such as achievable tolerance, is violated—EDAPS's planner reports the failure and the reason for the failure to the designers.

This generative process planning approach allows us to provide feedback about manufacturability, cost, and lead time to the designers, based on actual process plans for the manufacture of the device. Because manufacturing engineers are accustomed to a standard format for the specification of process plans, EDAPS's planner outputs the process plan in this format. See Figure 9.

5 USING THE SYSTEM

This section describes the interaction between the modules of the design environment, and the mechanism to integrate these modules into a single toolkit.

Designers and manufacturing engineers usually have different output requirements from the toolkit. For an electronic

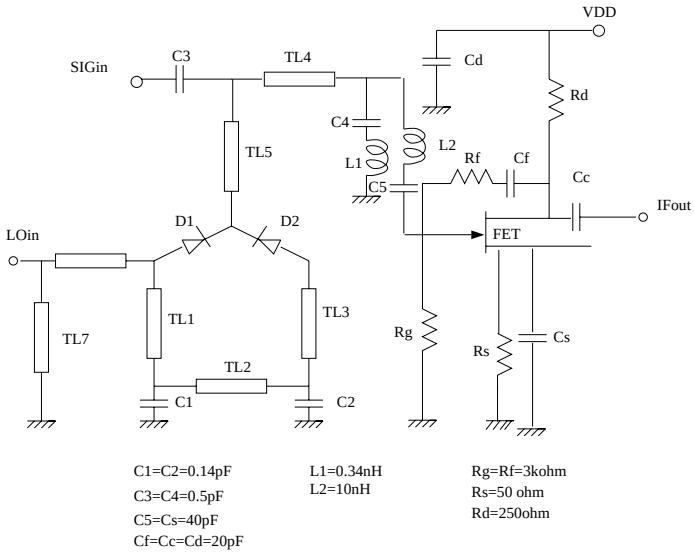

Figure 10. Mixer-IF amplifier schematic circuitry.

designer, the integration mechanism must be able to give feedback on the cost, quality, and lead times of process plans. It should also provide the designer information on the mechanical constraints such as the maximum board temperatures and size constraints on the design. However, for a mechanical designer, it should automatically generate shape description of the design. For a manufacturing engineer, process plans are the most important because that enables the designer to determine the ease of manufacturing the product and associated costs and lead times.

We provide the mechanism for the exchange of domain specific product attributes, with the ultimate objective of feeding back plan-based cost, quality and lead times to the designers. The integration, highlighted with an example, is explained below. It describes the steps which will usually be followed in designing a microwave module.

Step 1: Schematic Circuit—Circuit Schematic and Circuit Layout Module. The designer chooses the circuit schematic and layout module from the user interface. Libra is invoked. At this stage, the designer already understands the conceptual high-level design of the module and the different functional units that make it up. For the purpose of illustration, we use the example of a Mixer-IF amplifier circuitry [20] shown in Figure 10. The designer generates an initial network of circuitry based on device specifications, choosing hybrid packaged elements such as the resistors (R1, R2 and so forth), capacitors (C1, C2 and so forth), FETs, inductors (L1, L2 and so forth), and diodes (D1, D2), and distributed elements, such as the transmission lines (marked TL1, TL2 and so forth) from the library of parts supplied with Libra.

The designer then simulates the schematic circuit, yielding the response of the circuit to various forms of input. The design is monitored for functionality and noise levels. If the response is

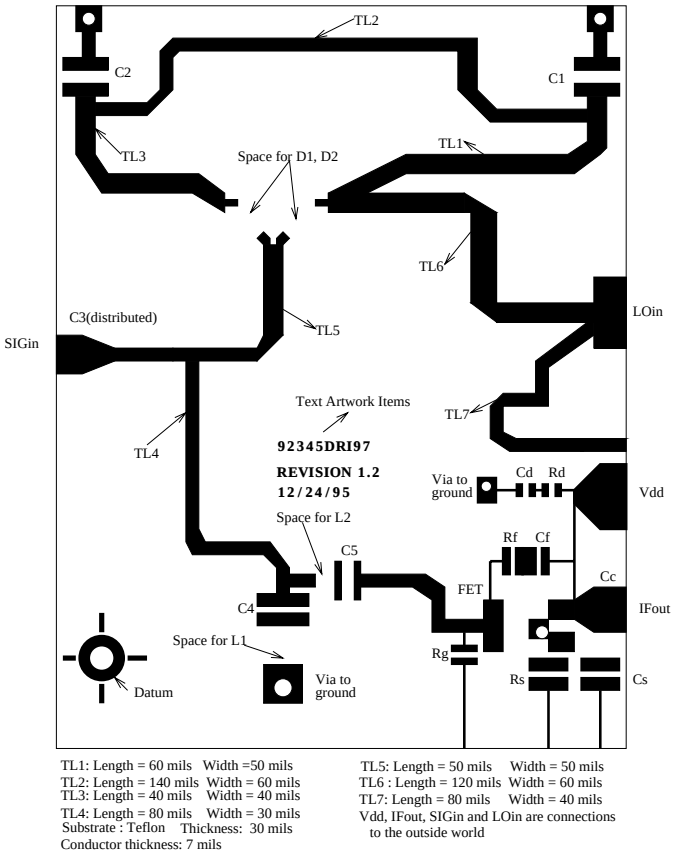

Figure 11. Mixer-IF amplifier circuitry layout.

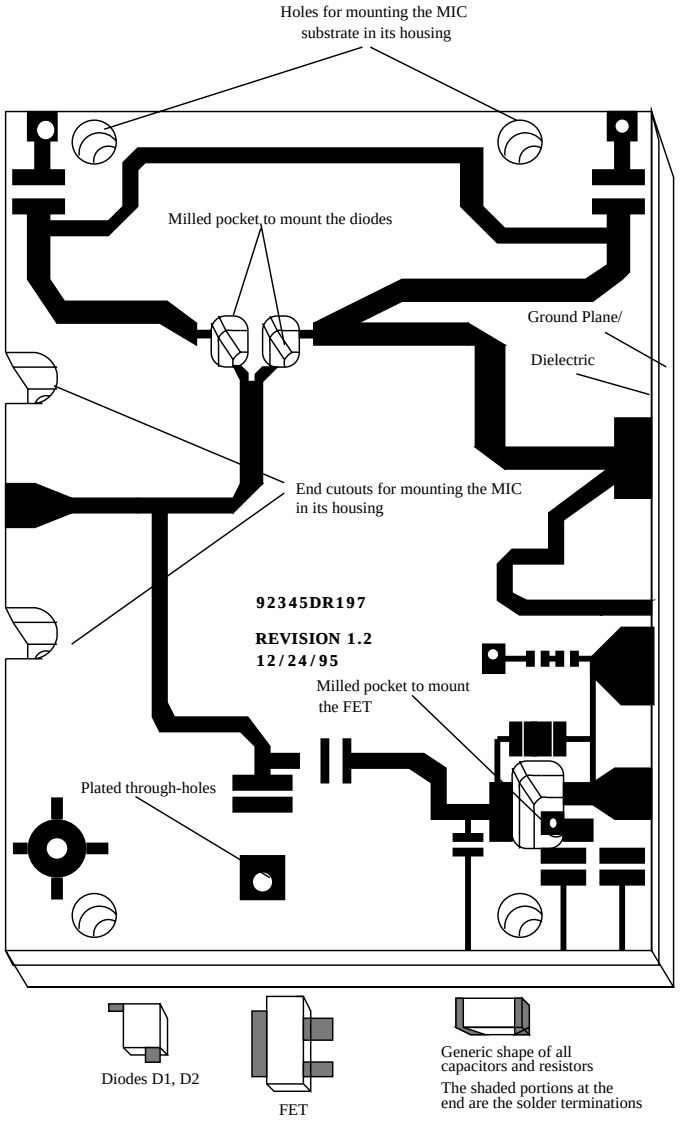

Figure 12. Development of mechanical features on the Mixer-IF amplifier substrate.

unsatisfactory, design modifications are made and re-simulated until a satisfactory design is obtained. The parameter values of all component, after circuit simulation, is listed in Figure 10.

Step 2 : Artwork Layout—Circuit Layout and Circuit Schematic Module. From within Libra, the designer then invokes ACADEMY for generating the layout of the circuitry. As mentioned earlier, artwork can either be automatically generated (e.g. for transmission lines) or manually specified. Figure 11 is the layout of the example circuitry. The user manually generates the text items and datum element. The artwork elements usually associated with hybrid packaged components are rectangular pads on which the components are soldered. Alternatively, the user can override default pad shape generation with user-defined shapes. In this example, the inductors are assumed to be coils, so that they can be soldered directly onto the capacitor pads that they are connected to. Therefore, gaps are left wherever inductors appear. Vias for grounding can also be seen in the layout.

Once artwork generation is completed, the system calls an application program that extracts the product information relevant for manufacturing, such as the substrate material (Teflon in this example), the dielectric thickness (30 mils), conductor thickness (7 mils), and so on, from the design database. This information is stored in C++ classes. Finally, the system translates the layout into an IGES file, and exports it to Microstation for substrate designing.

Step 3: Mechanical design—Substrate Design Module. Microstation is then invoked from the user interface. The Microstation kernel reads layout from the IGES file and re-generates the artwork as a Microstation design file. It then reads a file, where EDAPS stores location and dimensions of the packaged components, and using this information, displays the packaged components at their correct locations. Figure 12 illustrates some of the package shapes that will be generated by Microstation.

Microstation will then automatically generate milled pockets to mount components which have to be directly connected to the ground plane/heat sink. As can be seen in Figure 12, milled pockets for high-heat dissipating components—such as the diodes and the FET in the example—will be generated from the size information of their respective packages. The designer has the choice to override the mounting pocket generation feature of the system at any time, and can then either specify custom mounting pockets or not generate any mounting pocket at all. All other features—such as via holes, holes for clamping the MIC substrate, cutouts, and so forth—will be generated by the user at this stage in the mechanical substrate design module. As explained previously, milled pockets and drilled holes are stored as manufacturing features. Doing so eliminates the need for feature recognition to estimate machining times and cost.

When the mechanical design phase is complete, EDAPS stores information about the location, type, and dimensions of all machined features and packaged components in a file that is read by the process planner.

Step 4: Process Planner—Process Planning and Plan Evaluation Module. As we have mentioned, EDAPS's planner works by decomposing complex tasks into simpler tasks. The initial task, which decomposes into all other required tasks, is simply called "Make board".

Consider Figure 12. "Make board" decomposes into "Make plated through-holes and features"; "Make artwork"; "Assembly"; and "Testing and inspection". "Make plated through-holes and features" decomposes into "Drill plated through-holes"; "Plate plated through-holes"; and "Make features". "Drill plated through-holes" and "Plate plated through-holes" decompose into primitive tasks which we do not discuss here.

"Make features" is the next task, and because there are features left to be made, it decomposes into "Make a single feature", and "Make features". This "loop" in the task network allows us to decompose a task, such as "Make features", into zero or more subtasks, such as "Make a single feature".

"Make a single feature" decomposes into "Setup and end-mill (the top cutout on the left side of the substrate)", because in our planner, we always do all the milling before we do any drilling. "Setup and end-mill (the top cutout on the left side of the substrate)" decomposes into "Setup"; "Setup end-milling tool"; and "End mill". Because the part is not currently set up on the machining center, "Setup" decomposes into "Orient the part"; "Clamp the part"; and "Establish a datum point". All three of these tasks are primitive.

"Setup end-milling tool" is the next task, and because we just started, we assume that the correct end-milling tool is not installed on the machining center. Thus, this task decomposes into "Install end-milling tool (of the appropriate size)", which is a primitive task. Assuming tight tolerances, "End mill" decomposes into "Rough end-mill" and "Finish end-mill", both of which are primitive tasks.

"Make features" continues to decompose until a plan has been created for all five milling features and all thirteen drilling features. The next complex task is "Make artwork".

"Make artwork" decomposes into "Preclean for artwork"; "Apply photoresist"; "Artwork photolithography"; and "Etching". In our planner, all of these tasks but "Apply photoresist" are primitive. "Apply photoresist" has several alternative decompositions: "Spread photoresist from a spinner", or "Spindling the photoresist", or "Spraying the photoresist". "Apply photoresist" does **not** decompose into "Painting on the photoresist" in this case, because painting on the photoresist is not accurate enough for this substrate.

As mentioned before, because the method of application of photoresist does not affect anything else in the plan, EDAPS's planner will locally decide which photoresist application method is cheapest in this instance—"Spindling the photoresist", let us say—and will keep only that subtask in the plan.

The rest of the plan is generated in a similar manner, and output in the format shown in Figure 9. The output of the EDAPS planner includes:

- A totally ordered sequence of process specifications that can be used to produce the finished substrate from the materials given;
- Process parameters of all the processes that are required to manufacture the device;
- Estimates of cost and lead times.

The output can be fed back to the designers, with lead-time "hot spots" indicated. The designer can then choose to change the design elements, in order to reduce the lead time.

When the designers and manufacturing engineers are satisfied with the design, the artwork elements will be extracted out of Microstation, and the equivalent IGES file will be generated and sent to ACADEMY. ACADEMY can then export the design file in either IGES format or Gerber format for manufacturing.

6 CONCLUSIONS

In this paper we have described EDAPS, a design and process planning environment whose goal is to integrate mechanical and electronic design tools in a single platform, and to assist the designer in evaluating designs based on the manufacturing plans. The distinct advantage of such an approach is the ability to evaluate designs from the point of view of the designers and the manufacturers. EDAPS thus highlights a concurrent engineering approach that we have taken to reduce the lead times, and to improve the quality in electronic manufacturing.

EDAPS is still under development. To date, we have completed the routines to extract and store relevant manufacturing information from electronic designs, the routines that build the manufacturing features, and the process planning module. Work that remains to be done includes testing and fine-tuning of the

process planning knowledge base, performing trade-off analysis, providing feedback to the designers, and further consideration of the interactions between the designers and the process planner.

6.1 Lessons Learned So Far

Integration of Electrical and Mechanical Design. The ultimate solution to the problem of integrating electronic and mechanical design can be found in one of at least two ways. One possibility is the implementation of a single monolithic piece of code that includes both an electronic design subsystem and a solid modeling engine for mechanical design. The data structures in such an implementation would identify the solid model of a trace in the mechanical design with its function in the schematic of the electronic design. Such a solution would allow tightly coupled interaction between the electronic design subsystem and mechanical design subsystem—and could be used to generate sophisticated feedback to the designer, such as suggestions for how to change the proposed design to improve its manufacturability while maintaining acceptable performance. Unfortunately, such an approach requires the creation of a completely new system, which may be incompatible with the *legacy* systems already used in a factory.

Another possibility—the approach we have approximated in this experiment—is integrate existing systems for electrical and mechanical design. In addition, this approach requires extending the electronic design system to keep track of some of the information needed for mechanical design so that it will not be lost when users change the electrical design, and similarly extending the mechanical design system. The disadvantage of such a solution is that it may limit the interaction between the electronic design system and the solid modeler, and that in any case translating and transferring information from one system to another takes time and work. (In our system, because our feedback is based on the process plan for manufacturing, we didn't have to translate much information back to the electronic design system from the solid modeler.) However, such a solution allows companies to keep legacy systems in place; in addition, designers can change their electronic design system without changing their solid modeler, or vice versa.

Process Planning and Manufacturability Analysis. Most researchers have had great difficulty in developing generative process planners for complex mechanical parts, because the mechanical features have many interactions. However, generative process planning can be more easily applied to microwave modules, because the mechanical features have fewer interactions.

Hierarchical task-network planning appears to be an ideal approach for generative process planning in this domain. The decomposition in an HTN naturally corresponds to the decomposition of a MIC into the parts and processes required to manufacture it, and HTN's provide a unified framework that accommodates both electronic and mechanical manufacturing processes.

6.2 Future Work

In real life situations, designers never obtain a truly optimum design. A design that is optimal with respect to cost may have poor yields associated with it. In such cases, trade-offs have to be done to attain a design solution that is somewhat optimal with respect to all the decision variables.

We plan to incorporate a trade-off analysis module that gives the designer a clearer picture of all the cost versus quality trade-offs that are involved in each design. When finished, the planning module will construct a set of process plans, and will perform trade-off analysis on the plans to determine a set of pareto-optimal process plans, about which we can then provide feedback.

To do such trade-off analysis, we need models to predict yields, costs, and lead times. For costs, formulae are available from standard process handbooks. We can calculate lead times from the process plans.

However, yields are more difficult to predict. The simplest yield model associates a historically determined yield value with each component. Thus, component design features will have quality as an additional attribute. The fundamental assumption with this model is that yields are determined solely by components, and not by processes and the designs in which the components reside. In fact, all of processes, components and board design characteristics determine the yield of the microwave modules. Ball and others [3] consider such interactions between processes and parts, and solve the trade-off analysis as an integer programming problem. However, individual process-component yield values are required inputs for their models. For new designs, such as the ones we are considering, it is hard to predict such process-component yield values without having subjected the product to several runs in the production lines. We will determine the yield model most suitable for our application.

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