Problem Set #4

Quantum Error Correction
Instructor: Daniel Gottesman

Due Thursday, July 7, 2016

Problem #1. Teleportation of the controlled-phase gate

Let U be the gate

$$U = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & i \end{pmatrix}. \tag{1}$$

a) Find $UPU^\dagger$ for $P = X \otimes I$, $I \otimes X$, $Z \otimes I$, and $I \otimes Z$.

b) Find a *two-qubit* ancilla state and a circuit involving two data qubits and the ancilla consisting of Clifford group gates, Pauli basis measurements, and classical feed-forward, such that the output of the circuit is $U|\psi\rangle$. ($|\psi\rangle$ is the input state of the two data qubits.)

Problem #2. Correctness with weaker versions of fault tolerance

For this problem, we will consider a fault-tolerant protocol for a QECC capable of correcting t errors.

a) Suppose we consider weaker versions of the ECRP and the GPP. The weak ECRP has a $2s$-filter on the right-hand-side for the output instead of an s-filter when there are s faults in the EC gadget, with $2s \leq t$. The weak GPP (for a single-block gate) has an $(r + 2s)$-filter instead of an $(r + s)$-filter for the output on the right-hand-side when the input passes an r-filter and there are s faults in the circuit, with $r + 2s \leq t$. The correctness conditions are unchanged. For a single-block gate exRec, how many faults can we allow within the exRec and still guarantee that the exRec is correct?

b) Consider the weak version of the ECRP and a very weak version of the GPP, with a $(2r + 2s)$-filter for the output on the right-hand-side instead of a $(r + 2s)$-filter, for $2r + 2s \leq t$. With these properties, how many faults can we allow within the exRec and still guarantee that the exRec is correct?

Problem #3. Pseudo-thresholds

For this problem, use the FTEC circuit for the 7-qubit code for which we computed the threshold in class, which contains 64 CNOT locations and 104 single-qubit locations (waits, Hadamards, measurements, and $|0\rangle$ preparations), and again ignore corrections due to post-selection. Assume all single-qubit locations have the same error rate p_{single}, but CNOT locations may have a different error rate p_{CNOT}.

a) Write down formulas for the logical error rate (i.e., after level reduction) for a single level of the 7-qubit code for logical CNOT and logical single-qubit locations in terms of p_{single} and p_{CNOT}. Lump together different types of single-block extended rectangles; the largest single-block extended rectangle is for the Hadamard.

b) Now imagine that the physical error rate for single-qubit locations is $p_{\text{single}} = 0$. Calculate the *pseudo-threshold* for CNOT gates: p_{PT} is the CNOT error rate at which the logical CNOT error rate after one level of the QECC is less than or equal to p_{CNOT}.

c) Show that after two levels of concatenation, the logical CNOT error rate is greater than p_{PT} when the error rates on physical locations are $p_{\text{single}} = 0$, $p_{\text{CNOT}} = p_{\text{PT}}$.