Reading for this week:

Mano Chapter 5 to section 5-4

Homework #5 was handed out

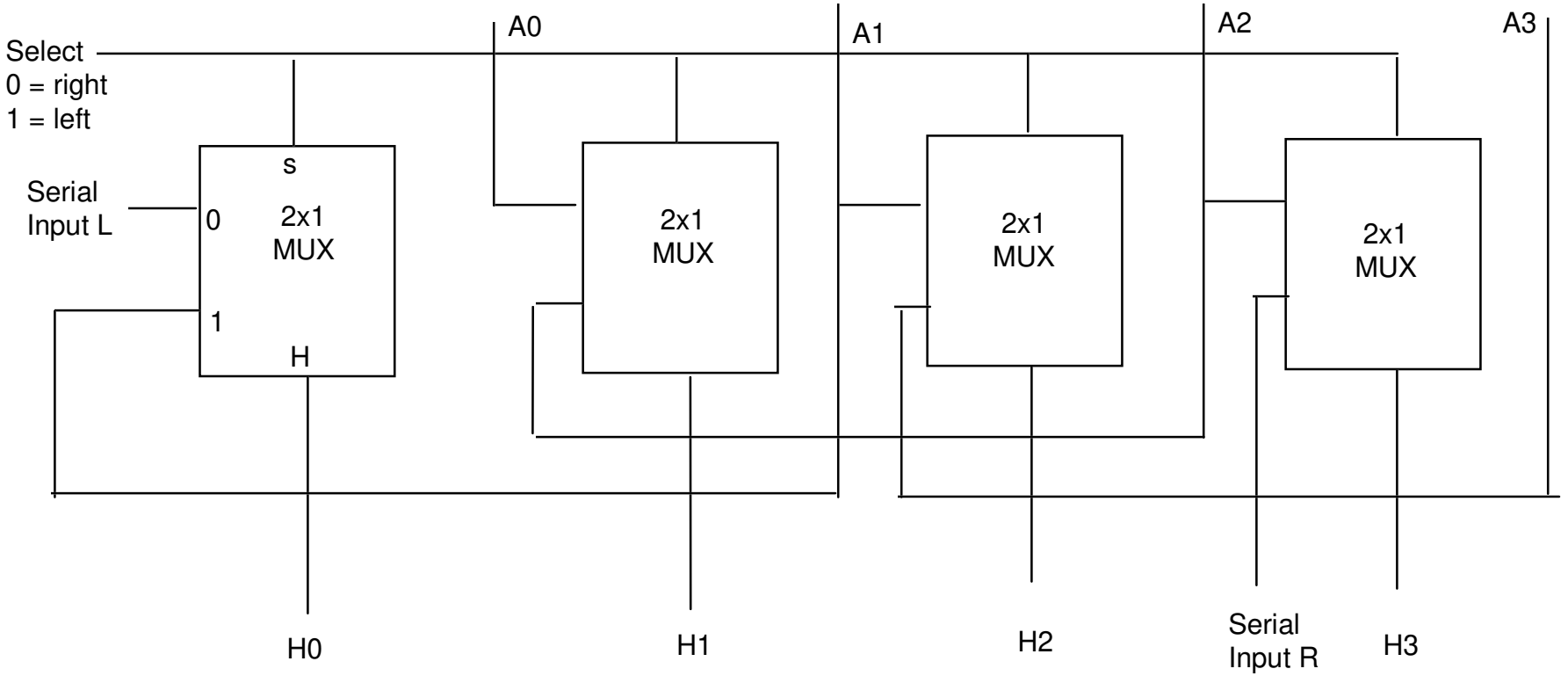
The Midterm was returned

Shift Microoperations

- Shift bits within a register
- Logical shift
  - left shift R1 $\leftarrow$ shl R1
  - right shift R2 $\leftarrow$ shr R2
  - zero is shifted in
- Circular Shift
  - left circular shift R1 $\leftarrow$ cil R1
  - right circular shift R1 $\leftarrow$ cir R1
- Arithmetic Shift
  - leaves sign bit unchanged
  - provides multiply and divide by 2
  - left (multiply) R1 $\leftarrow$ ashl R1
  - right (divide) R1 $\leftarrow$ ashr R1

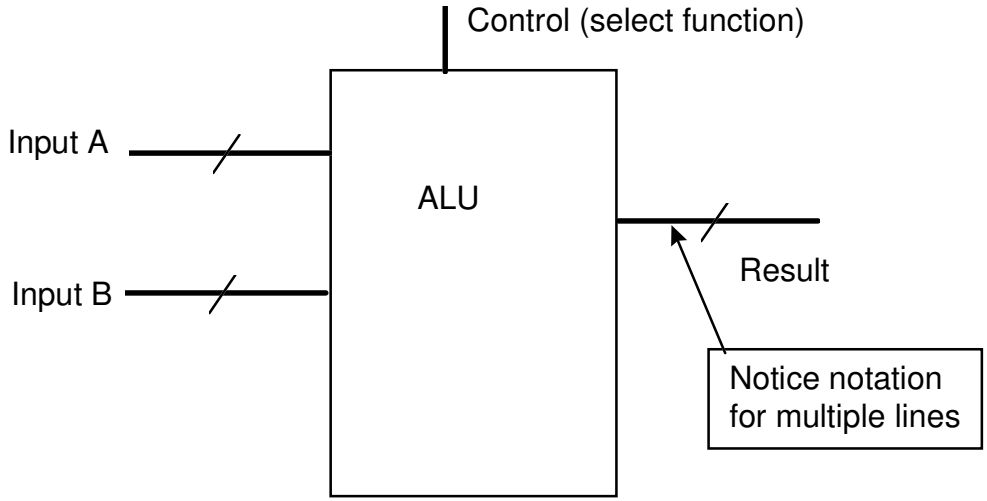
Building a Shifter

- Could use shift register
  - requires each register to be able to shift
  - use a shared shift register (but would require time to load)
- Alternative is to build a standalone shifter
  - can use multiplexors for this



Arithmetic Logic Unit (ALU)

- Combines arithmetic and logic functions together
- A shared resource for operating on data



- How can we attach an ALU to registers
  - with one bus need to have special registers
  - use two buses (more expensive, but faster)

ALU Functions

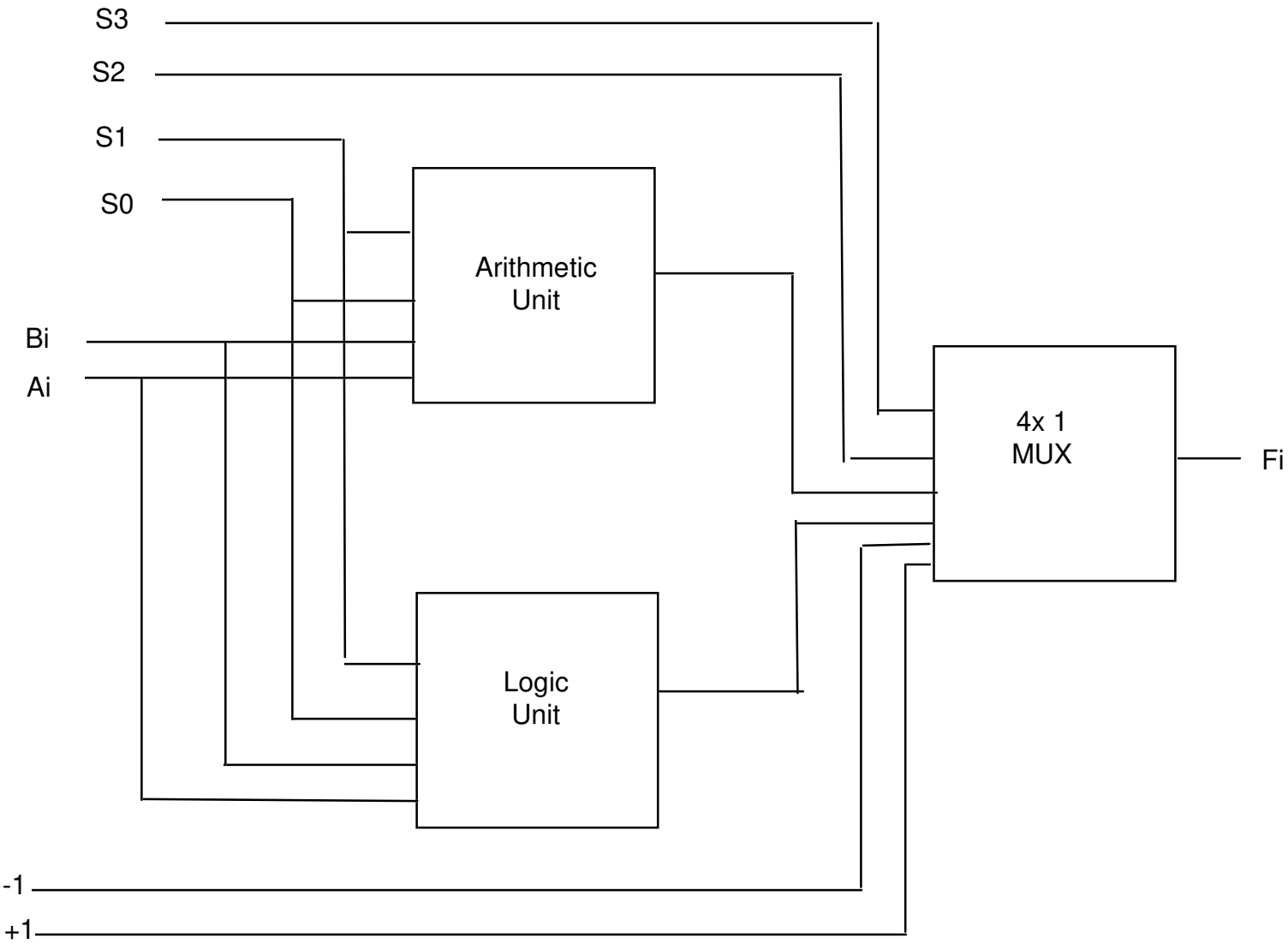
- Combine Arithmetic and logic units from before

Note this table is correct, but there is an error in table 4-8 in the book.

S3	S2	S1	S0	Cin	Operation	Function
0	0	0	0	0	F = A + B	
0	0	0	0	1	F = A + B + 1	
0	0	0	1	0	F = A + B’	
0	0	0	1	1	F = A - B	
0	0	1	0	0	F = A	
0	0	1	0	1	F = A + 1	
0	0	1	1	0	F = A -1	
0	0	1	1	1	F = A	
0	1	0	0	x	F = A ^ B	
0	1	0	1	x	F = A v B	
0	1	1	0	x	F = A (+) B	
0	1	1	1	x	F = A’	
1	0	x	x	x	F = shr A	
1	1	x	x	x	F = shl A	

Building the ALU

- Use Previous parts!



Exam Results

- Average 57
  - appeals will likely raise this a bit
- Low 22, high 90, SD 16.1
  - in the past one, SD above avg.. was an A
  - one SD below average has been an F
  - students dropping the class will raise the average
- Rules of Engagement for Re-grading
  - Mandatory overnight waiting period.
  - If you submit a question for re-grading, I reserve the right to regrade the **entire** exam.

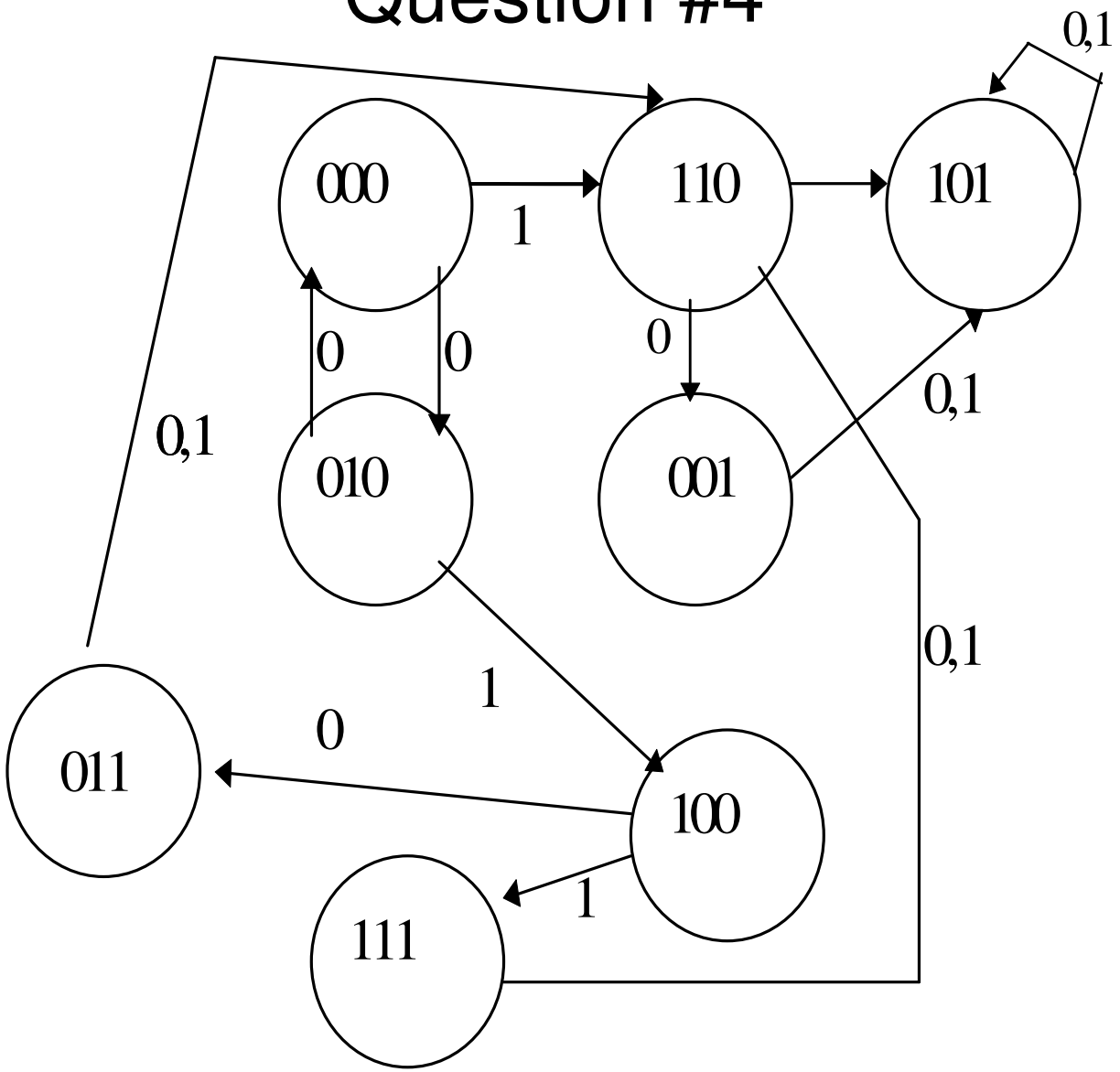
Exam Results by Question

Question	1	2	3	4	5	6
Max	14	9	2	9	14	8
Min	10	2	0	0	0	0
Avg	15	10	12	20	20	20

Question #3

- Each state Table
  - 4 FF's imply 16 states
  - 2 inputs means 4 possible input patterns
  - therefore there are 64 lines in each state table
- Possible state tables (wo output)
  - each line can transition to one of 16 possible states
  - therefore there are 16^{64} possible tables
- Output
  - output is a function on current state alone so each of the 16 states can produce a 0 or a 1
  - therefore there are 2^{16} possible outputs per state table
- Overall
  - 16^{64} possible tables times 2^{16} outputs = 2^{262}

Question #4



Question #5

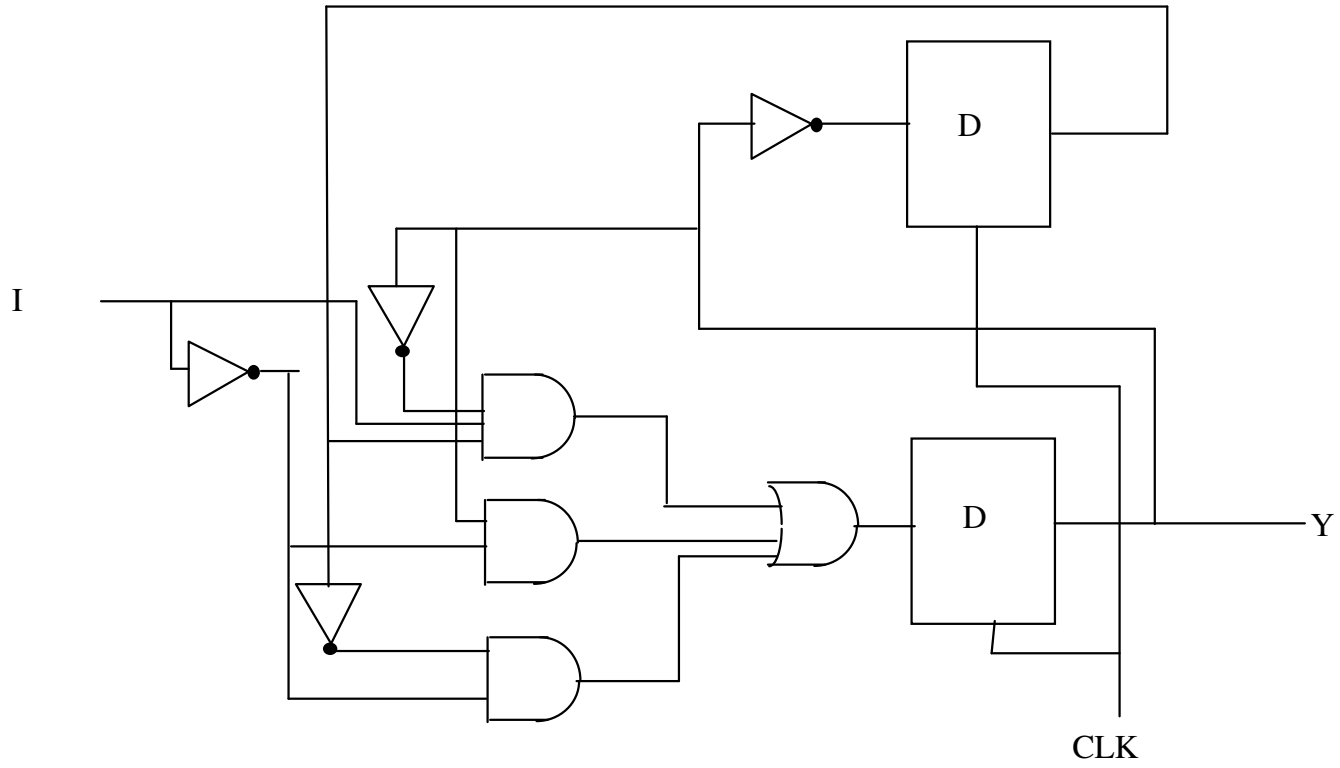
- Common errors
  - missed circling around the corner of the K-map for D1
  - output is a function of current state
  - forgot to show the clock

S1	00	01	11	10
0	1	0	1	1
1	0	1	0	0

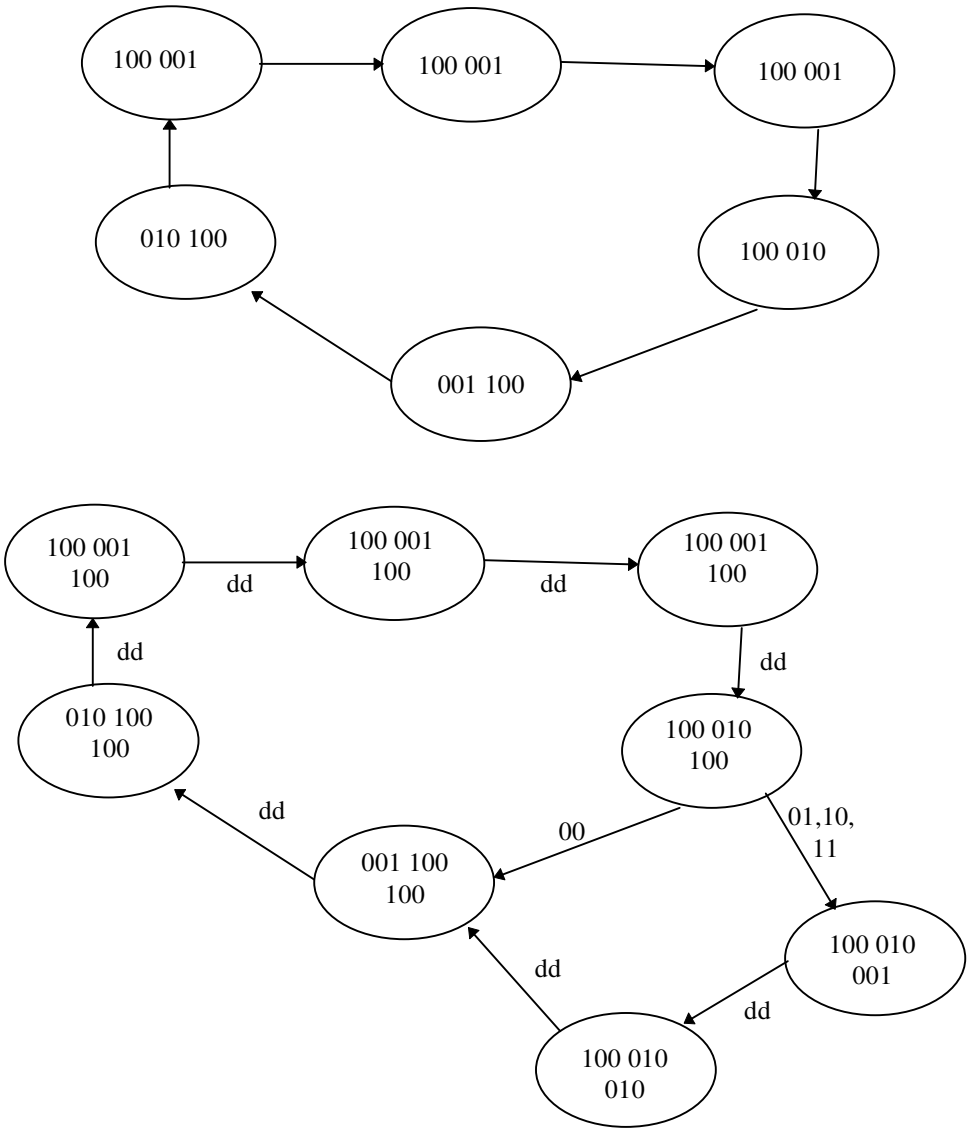
S0	00	01	11	10
0	1	1	0	0
1	1	1	0	0

Y	00	01	11	10
0	0	0	1	1
1	0	0	1	1

Question 5 (cont)



Question #6


100 001
100 001
100 001
010 100
100 010
001 100
100 001 100
dd
100 001 100
dd
100 001 100
dd
010 100 100
dd
100 010 100
dd
00
01,10, 11
001 100 100
dd
100 010 001
dd
100 010 010